REMARKS

Claims 1-6 and 14-16 are active in the present application. Claims 1, 2 and 5 have been amended and claims 14-16 have been cancelled. No new matter has been added by the amendment. Entry of the Amendment is respectfully requested, as the Amendment places the application in condition for allowance. Accordingly, reconsideration and allowance of the application are respectfully requested.

Claims 1 and 3-6 were rejected under 35 USC §102(e) as anticipated by US Patent No. 6,480,892 (Levay). Applicants respectfully traverse the rejection.

Claim 1 includes two hardware elements, a protocol processor and a CPU. The protocol processor is a hardware element, as evidenced at page 3, lines 26-29 of the specification, where it is stated that the protocol processor preferably is a RISC processor. Levay only discloses a software packet filter and not a separate processor for performing packet handling.

Claims 1 and 5 have been amended to recite that the protocol processor is a RISC processor. In view thereof, claims 1 and 3-6 are not anticipated by Levay. Accordingly, Applicants respectfully request that the rejection of claims 1 and 3-6 be withdrawn.

Claims 2 and 14-16 were rejected under 35 USC §103 as unpatentable over Levay in view of US Patent Application No. 2001/0043614 (Viswanadham). The Office Action states that Levay discloses an apparatus and method for processing IP/RTP packets, and that Viswanadham discloses the use of a RISC processor and dual port memory. Claims 1 and 4 have been amended to include the subject matter of claims 2 and 14, and 15-16, respectively. Thus, as the rejection would

apply to pending claims 1-6, Applicants respectfully traverse the rejection.

Viswanadham discloses a switch element 22 that includes a Network Management processor (NMP) 10 and a Route/Switch (RS) processor 12, both of which are RISC processors, for providing standards-based dynamic routing and non-real time activities (Viswanadham at [0027]). The NMP processor 10 and the RS processor 12 are coupled to each other with a switch ASIC 20 (Viswanadham at [0025]. As shown in FIG. 3, the ASIC 20 is coupled to the external 16 and manages all memory access by the RS processor 12.

Contrary to what's stated the in the Office Action, it is not at all apparent that Viswanadham teaches using a dual port memory for communications between the NMP processor 10 and the RS processor 12, and such feature, where not shown or discussed, should not be read into the disclosure.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application, including claims 1-6, is in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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